Amendments to the Specification:

Please replace the paragraph at page 4, beginning at line 12 with the following:

The microcontroller M preferably includes an internal bus 100 coupling, an execution unit 124, system peripherals 174, memory peripherals 176 and serial communication peripherals 172. The execution unit 124 in the disclosed embodiment is compatible with the Am186 instruction set implemented in a variety of microcontrollers from Advanced Micro Devices, Inc., of Sunnyvale, California. A variety of other execution units could be used instead of the execution unit 124. The system peripherals 174 include a ~~watch-dog~~ watchdog timer (WDT) 104 for generating non-maskable interrupts (NMIs), microcontroller resets, and system resets. An interrupt controller 108 for supporting thirty-six maskable interrupt sources through the use of fifteen channels is also provided as a system peripheral. One disclosed system peripheral is a three-channel timer control unit 112. The timer control unit 112 includes three 16-bit programmable timers. Another system peripheral is a general-purpose direct memory access (DMA) unit 116 with four channels 0-3. A programmable I/O unit 132 of the microcontroller M supports user programmable input/output signal (PIOs). In the disclosed embodiment, forty-eight PIOs are provided.

Please replace the paragraph at page 9, beginning at line 31 and continuing on page 10 with the following:

Provided below is exemplary hardware description code (in this case, Verilog RTL (Register Transfer Level)) for the clock switching circuit of Figure [[1]]2a, along with a table providing general descriptions for the variables within the code. Those skilled in the art will readily relate and correlate the table and code below with the other disclosure provided herein. It should be apparent to those skilled in the art that other implementations of the clock switching circuit are possible.

Please replace the paragraph at page 11, beginning at line 33 and continuing on page 12 with the following:

Figures 3-5 are timing diagrams showing the effect of injection of glitches into a circuit constructed according to the synthesization as shown in Figure 2b. Figure 3 is a timing diagram for an embodiment where CLK1 has a lower frequency than CLK2. Signal n226 is a buffered version of signal CLK1. Likewise, signal n223 is a buffered version of

signal CLK2 that has been passed through inverters 210 and 212. Signal meta_clk1_enb126 shows the output of AND gate 112. Signal meta_clk1_sel51 shows the output of OR gate 122. Signal meta_clk1_enb shows the output signal from flip-flop 114, which is connected to the D0 input of flip-flop 116. Signal meta_clk1_sel is the output of flip-flop 124, which is connected to the input D0 of flip-flop 126. As can be seen in Figure 3, the initial blackened areas of the CLKOUT signal are in an unknown state because the flip-flops 114-116 and 124-126 have not been reset. Likewise, the blackened areas of signals meta_clk1_sel51, meta_clk1_enb, meta_clk1_sel, sync_clk1_enb, and sync_clk1_sel indicate that the status of those signals are is unknown because the flip-flops 114-116 and 124-126 have not been reset. Figure 3 shows 2ns (nanosecond) glitches on the CLK_SEL signal injected at the capturing edge of both CLK1 and CLK2. These glitches violate the setup or hold time of the synchronizing flip-flops 114 and 124 in upper and lower synchronization stages 120 and 110, respectively. Glitch 310 is a positive going 2ns glitch. In this case, it can be seen that CLKOUT did not glitch and CLKOUT tracked CLK2 correctly with an additional one CLK2 period of "low stretch" (i.e., staying in a low state for an additional length of time) introduced because the circuit was resolving the glitch 310, due to the sync_clk1_sel signal being asserted high for one CLK2 period.